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Case Docket No. 98GR22045417

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Transmitted herewith for filing is the patent application of:

Inventors: **Christophe GARNIER, Pascal DEBATY**

For: **VOLTAGE RAMP GENERATOR AND CURRENT RAMP GENERATOR
INCLUDING SUCH A GENERATOR**

Enclosed are:

- (X) Patent Application: 13 pages, 8 claims.
- (X) 3 Sheets of drawings.
- () A certified copy of _____ application.
- () Citation Under 37 CFR 1.97 and PTO-1449.
- (X) Preliminary Amendment.
- (X) Submission of Proposed Drawing Modification.

The Declaration and Filing Fee are **NOT ENCLOSED**.

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PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
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Sir:
Prior to the calculation of fees and examination of
the present application, please enter the amendments and
remarks set out below.

In the Drawings:

Submitted herewith is a request for a proposed
drawing modification as indicated in red ink to label FIG. 1
as prior art.

In the Claims:

Cancel Claims 1-8.

Add new Claims 9-40.

9. A voltage ramp generator comprising:

a capacitance; and

a charging circuit connected to said capacitance and

comprising

In re Patent Application of
GARNIER ET AL.
Serial No. Not Yet Assigned
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a current generator having a first resistance,
and

a circuit connected to said current generator
and to said capacitance comprising a second
resistance and enabling a capacitance charging
current to be proportional to a square of a ratio of
the second resistance and the first resistance.

10. A voltage ramp generator according to Claim 9,
wherein said charging circuit comprises a degenerate current
mirror circuit.

11. A voltage ramp generator according to Claim 10,
wherein said degenerate current mirror circuit comprises:

a first MOS transistor having a channel of a first
conductivity type comprising a gate, a drain and a source, the
drain and the gate being connected to said current generator,
and the source being connected to said second resistance; and

a second MOS transistor having a channel of the
first conductivity type comprising a gate, a drain and a
source, the gate being connected to the gate of said first MOS
transistor, the source being connected to a supply voltage,
and the drain being connected to said capacitance.

12. A voltage ramp generator according to Claim 11,
wherein each of said first and second MOS transistors
comprises a P-channel MOS transistor.

13. A voltage ramp generator according to Claim 9,
wherein said capacitance comprises a gate capacitance of a MOS
transistor.

In re Patent Application of
GARNIER ET AL.
Serial No. Not Yet Assigned
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14. A voltage ramp generator according to Claim 9, wherein current generated by said current generator is based upon the equation:

$$I_{g2} = K2 \times \frac{V_{g2}}{R_{g2}}$$

where I_{g2} is the current, $K2$ is a proportionality coefficient, R_{g2} is the first resistance, and V_{g2} is a

reference voltage proportional to the quantity $k \frac{T}{q}$, where k is the Boltzmann constant, T is absolute temperature, and q is the charge of an electron.

15. A voltage ramp generator comprising:
a capacitance; and
a charging circuit connected to said capacitance and comprising

a current generator, and
a degenerate current mirror circuit connected to said current generator and to said capacitance for generating a capacitance charging current.

16. A voltage ramp generator according to Claim 15, wherein said current generator has a first resistance, and said degenerate current mirror circuit has a second resistance such that the capacitance charging current is proportional to a square of a ratio of the second resistance and the first resistance.

In re Patent Application of
GARNIER ET AL.
Serial No. **Not Yet Assigned**
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17. A voltage ramp generator according to Claim 15, wherein said degenerate current mirror circuit comprises:

a first MOS transistor having a channel of a first conductivity type comprising a gate, a drain and a source, the drain and the gate being connected to said current generator, and the source being connected to said second resistance; and

a second MOS transistor having a channel of the first conductivity type comprising a gate, a drain and a source, the gate being connected to the gate of said first MOS transistor, the source being connected to a supply voltage, and the drain being connected to said capacitance.

18. A voltage ramp generator according to Claim 17, wherein each of said first and second MOS transistors comprises a P-channel MOS transistor.

19. A voltage ramp generator according to Claim 15, wherein said capacitance comprises a gate capacitance of a MOS transistor.

20. A voltage ramp generator according to Claim 15, wherein current generated by said current generator is based upon the equation:

$$I_{g2} = K_2 \times \frac{V_{g2}}{R_{g2}}$$

where I_{g2} is the current, K_2 is a proportionality coefficient, R_{g2} is the first resistance, and V_{g2} is a

reference voltage proportional to the quantity $k \frac{T}{q}$, where k is

In re Patent Application of
GARNIER ET AL.
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the Boltzmann constant, T is absolute temperature, and q is the charge of an electron.

21. A current ramp generator comprising:
a voltage ramp generator comprising
a capacitance, and
a charging circuit connected to said
capacitance and comprising
a current generator having a first
resistance, and
a circuit connected to said current
generator and to said capacitance comprising a
second resistance and enabling a capacitance
charging current to be proportional to a square
of a ratio of the second resistance and the
first resistance; and
a conversion circuit connected to said voltage ramp
generator for generating a current ramp.

22. A current ramp generator according to Claim 21,
wherein said conversion circuit comprises a third resistance.

23. A current ramp generator according to Claim 21,
wherein said third resistance comprises an implanted
resistance having a positive temperature coefficient.

24. A current ramp generator according to Claim 21,
wherein said charging circuit comprises a degenerate current
mirror circuit.

25. A current ramp generator according to Claim 24,
wherein said degenerate current mirror circuit comprises:

In re Patent Application of
GARNIER ET AL.
Serial No. Not Yet Assigned
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a first MOS transistor having a channel of a first conductivity type comprising a gate, a drain and a source, the drain and the gate being connected to said current generator, and the source being connected to said second resistance; and

a second MOS transistor having a channel of the first conductivity type comprising a gate, a drain and a source, the gate being connected to the gate of said first MOS transistor, the source being connected to a supply voltage, and the drain being connected to said capacitance.

26. A current ramp generator according to Claim 25, wherein each of said first and second MOS transistors comprises a P-channel MOS transistor.

27. A current ramp generator according to Claim 21, wherein said capacitance comprises a gate capacitance of a MOS transistor.

28. A current ramp generator according to Claim 21, wherein current generated by said current generator is based upon the equation:

$$I_{g2} = K2 \times \frac{V_{g2}}{R_{g2}}$$

where I_{g2} is the current, $K2$ is a proportionality coefficient, R_{g2} is the first resistance, and V_{g2} is a

reference voltage proportional to the quantity $k \frac{T}{q}$, where k is the Boltzmann constant, T is absolute temperature, and q is the charge of an electron.

In re Patent Application of
GARNIER ET AL.
Serial No. Not Yet Assigned
Filed: Herewith

29. A current ramp generator comprising:
a voltage ramp generator comprising
a capacitance, and
a charging circuit connected to said
capacitance and comprising
a current generator, and
a degenerate current mirror circuit
connected to said current generator and to said
capacitance for generating a capacitance
charging current; and
a third resistance connected to said voltage ramp
generator for generating a current ramp.

30. A current ramp generator according to Claim 29,
wherein said current generator has a first resistance, and
said degenerate current mirror circuit has a second resistance
such that the capacitance charging current is proportional to
a square of a ratio of the second resistance and the first
resistance.

31. A current ramp generator according to Claim 29,
wherein said third resistance comprises an implanted
resistance having a positive temperature coefficient.

32. A current ramp generator according to Claim 29,
wherein said degenerate current mirror circuit comprises:
a first MOS transistor having a channel of a first
conductivity type comprising a gate, a drain and a source, the
drain and the gate being connected to said current generator,
and the source being connected to said second resistance; and
a second MOS transistor having a channel of the
first conductivity type comprising a gate, a drain and a

In re Patent Application of
GARNIER ET AL.
Serial No. **Not Yet Assigned**
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source, the gate being connected to the gate of said first MOS transistor, the source being connected to a supply voltage, and the drain being connected to said capacitance.

33. A current ramp generator according to Claim 32, wherein each of said first and second MOS transistors comprises a P-channel MOS transistor.

34. A current ramp generator according to Claim 29, wherein said capacitance comprises a gate capacitance of a MOS transistor.

35. A current ramp generator according to Claim 29, wherein current generated by said current generator is based upon the equation:

$$I_{g2} = K2 \times \frac{V_{g2}}{R_{g2}}$$

where I_{g2} is the current, $K2$ is a proportionality coefficient, R_{g2} is the first resistance, and V_{g2} is a

reference voltage proportional to the quantity $k \frac{T}{q}$, where k is the Boltzmann constant, T is absolute temperature, and q is the charge of an electron.

36. A method for generating a ramp voltage comprising the steps of:

generating a capacitance charging current using a charging circuit comprising a current generator having a first resistance and a circuit connected to the generator comprising

In re Patent Application of
GARNIER ET AL.
Serial No. Not Yet Assigned
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a second resistance for enabling the capacitance charging current to be proportional to a square of a ratio of the second resistance and the first resistance; and

charging a capacitance with the capacitance charging current for generating the ramp voltage.

37. A method according to Claim 36, wherein the circuit comprises a degenerate current mirror circuit.

38. A method according to Claim 37, wherein the degenerate current mirror circuit comprises:

a first MOS transistor having a channel of a first conductivity type comprising a gate, a drain and a source, the drain and the gate being connected to said current generator, and the source being connected to said second resistance; and

a second MOS transistor having a channel of the first conductivity type comprising a gate, a drain and a source, the gate being connected to the gate of said first MOS transistor, the source being connected to a supply voltage, and the drain being connected to said capacitance.

39. A method according to Claim 36, wherein the capacitance comprises a gate capacitance of a MOS transistor.

40. A method according to Claim 36, wherein current generated by the current generator is based upon the equation:

$$I_{g2} = K2 \times \frac{V_{g2}^2}{R_{g2}}$$

where I_{g2} is the current, $K2$ is a proportionality coefficient, R_{g2} is the first resistance, and V_{g2} is a

In re Patent Application of
GARNIER ET AL.
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reference voltage proportional to the quantity $k\frac{T}{q}$, where k is the Boltzmann constant, T is absolute temperature, and q is the charge of an electron.

REMARKS

It is believed that all of the claims are patentable over the prior art. Accordingly, after the Examiner completes a thorough examination and finds the claims patentable, a Notice of Allowance is respectfully requested in due course. Should the Examiner determine any minor informalities that need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number below.

Respectfully submitted,

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VOLTAGE RAMP GENERATOR AND CURRENT RAMP GENERATOR INCLUDING SUCH A GENERATOR

Field of the Invention

The present invention relates to a voltage ramp generator, and to a current ramp generator that converts the voltage ramp generator into the current
5 ramp generator. The present invention has a particularly advantageous application for DC voltage converters operating in a current mode, for example.

Background of the Invention

Circuits for DC voltage converters operating
10 in a current mode include a regulation circuit that includes a current ramp generator necessary to stabilize the regulation circuit. It is therefore necessary for the current ramp generator to have only slight component and temperature variations.

15 A current ramp generator in accordance with the prior art is shown in Figure 1. The current ramp generator is made up of a voltage ramp generator circuit and a circuit that enables the voltage ramp to be converted into a current ramp. The voltage ramp
20 generator circuit is made up of a current generator I_{g1} and a capacitance C . The current I_{g1} charges the capacitance C in accordance with the equation:

$$\frac{\Delta V_c}{\Delta t} = \frac{1}{C} \times I_{g1}$$

where V_c is the voltage at the terminals of the capacitance C .

As is known to those skilled in the art, the current I_{g1} can be written as:

5
$$I_{g1} = K1 \times \frac{V_{g1}}{R_{g1}}$$

where V_{g1} is a reference voltage such as a Bandgap voltage, for example, and R_{g1} is the resistance of the current generator, and $K1$ is a proportionality coefficient.

10 The circuit permits the conversion of the voltage ramp into a current ramp, and is made up of an operational amplifier A, three transistors T1, T2, T3 and a resistance R_s . The operational amplifier A includes a first input (e-), a second input (e+) and an
15 output. The transistor T1 is a N-type MOS transistor including a gate, a source and a drain, and the transistors T2 and T3 are P-type MOS transistors, each including a gate, a source and a drain.

The first input (e-) of the operational
20 amplifier A is connected to the source of the transistor T1. The gate of which is connected to the output of the operational amplifier A, and the drain is connected to the drain of transistor T2. The second input (e+) of the operational amplifier A is connected
25 to the first terminal of the capacitance C . The second terminal the capacitance C is connected to ground. The source of transistor T1 is connected to the first terminal of the resistance R_s , and the second terminal of which is connected to ground.

30 The transistors T2 and T3 are assembled as a current mirror. The source of transistor T2 is connected to a supply voltage V_+ . The drain and the gate of transistor T2 are connected to one another and to the gate of transistor T3. The source of transistor
35 T3 is connected to the supply voltage V_+ , and the drain

is connected to the circuit (not shown in the figure) which collects the current I_s . Variation of the current I_s is in relation to time which forms the current ramp.

- 5 In a known way, the variation of the current I_s in relation to time is given by the equation:

$$\frac{\Delta I_s}{\Delta t} = \frac{1}{C} \times \frac{V_{g1}}{R_{g1}} \times K1 \times \frac{1}{R_s}$$

It follows that the variation of the gradient

- 10 $\frac{\Delta I_s}{\Delta t}$ depends directly on the variations of resistances R_{g1} and R_s and of the capacitance C . The resistances R_{g1} and R_s can have a spread on the order of $\pm 20\%$. These spreads are then reflected in the current ramp on the order of $\pm 40\%$.

- 15 Prior approaches for correcting the current ramp spreads include adjusting the resistance R_s . It is then necessary to use a sequence of tests to adjust the value of resistance R_s . Provision is thus made to use fuse type memory points to adjust the ramp of each
20 circuit. This adjustment is a tedious operation. Furthermore, the design of the resistance R_s produced as a combination of fuses requires a relatively large area of the circuit.

- In addition, resistances R_{g1} and R_s have
25 temperature variations. These variations also have an impact on the current ramp. Since the adjustment of resistance R_s is only valid at the temperature at which it is carried out, the temperature dependence is not corrected.

Background of the Invention

In view of the foregoing background, the present invention does not have the above described disadvantages. In effect, the invention relates to a
5 voltage ramp generator comprising a capacitance and a charging circuit that permits the generation of a charging current for the capacitance. The charging circuit for the capacitance comprises a current generator of resistance R_{g2} . The charging circuit for
10 the capacitance includes means that permit the charging current for the capacitance to be proportional to $(R_e/R_{g2})^2$, where R_e is a resistance.

According to one particularly advantageous embodiment of the invention, the means that permit the
15 charging current for the capacitance to be proportional to the quantity $(R_e/R_{g2})^2$ comprises a degenerate current mirror. The term degenerate current mirror is used to mean a current mirror whose current ratio is not equal to the ratio of the surface areas of the MOS
20 transistors that makes it up.

The invention also relates to a current ramp generator comprising a voltage ramp generator and a circuit that permits the conversion of the voltage ramp to a current ramp. The voltage ramp generator is a
25 voltage ramp generator such as the one mentioned above.

According to the preferred embodiment of the invention, the components forming the voltage ramp generator and the current ramp generator are produced using CMOS technology. The invention also relates to
30 where the components are produced using a different technology, such as bipolar technology, for example.

Brief Description of the Drawings

Other characteristics and advantages of the invention will become apparent on reading a description
35 of a preferred embodiment of the invention made making reference to the appended figures among which:

Figure 1 shows a current ramp generator according to the prior art,

Figure 2 shows a voltage ramp generator according to the preferred embodiment of the present invention, and

Figure 3 shows a current ramp generator according to the preferred embodiment of the present invention.

Detailed Description of the Preferred Embodiments

10 In all the figures, the same reference numbers designate the same components. Figure 2 represents a voltage ramp generator according to the preferred embodiment of the present invention. The voltage ramp generator circuit includes a current
15 generator Ig2, a resistance Re, a capacitance C and two P-type MOS transistors T4 and T5 each comprising a gate, a drain and a source.

The transistor T4 has its source connected to a first terminal of the resistance Re, the second
20 terminal of which is connected to a supply voltage V+. The drain and the gate of transistor T4 are connected to a first terminal of the current generator Ig2, the second terminal of which is connected to ground. The transistor T5 has its gate connected to the gate of
25 transistor T4, its source connected to the supply voltage V+ and its drain connected to a first terminal of the capacitance C. The second terminal of the capacitance C is connected to ground.

Preferably, the substrate effect is
30 suppressed on transistors T4 and T5, and the voltage threshold Vth4 of transistor T4 is equal to the voltage threshold Vth5 of transistor T5. Current Ig2 passes through the resistance Re. Therefore, it follows that:

$$Re \times Ig2 + VGST4 - Vth4 = VGST5 - Vth5,$$

where VGST4 is the gate/source voltage of transistor T4 and VGST5 is the gate/source voltage of transistor T5.

According to the invention, the resistance Re
5 is chosen in such a way that:

$$Re \times Ig2 \gg VGST4 - Vth4,$$

It follows therefore:

$$VGST5 - Vth5 \neq Re \times Ig2,$$

In CMOS technology, the current which passes
10 through the transistor T5 is written as:

$$I_{T5} = \frac{\mu \times Cox}{2} \times \frac{W}{L} \times (V_{GST5} - Vth5)^2,$$

where μ is the mobility of the carriers, Cox
is the gate capacitance of the transistor T5, W is the
channel width of transistor T5, L is the channel length
15 of transistor T5.

It follows, therefore, that:

$$I_{T5} = \frac{\mu \times Cox}{2} \times \frac{W}{L} \times (Re \times Ig2)^2,$$

The current Ig2 can be written as:

$$Ig2 = K2 \times \frac{Vg2}{Rg2},$$

20 where Vg2 is a reference voltage, Rg2 is the
resistance of the current generator and K2 is a
proportionality coefficient.

Preferably, the voltage V_{g2} is proportional to the quantity $k\frac{T}{q}$, where k is the Boltzmann constant, T is absolute temperature and q is the charge of an electron.

5 It follows, therefore, that:

$$I_{T5} = \frac{\mu \times Cox}{2} \times \frac{W}{L} \times \left(\frac{Re}{Rg2} \right)^2 \times K2^2 \times Vg2^2.$$

The current I_{T5} is the current which charges the capacitance C . The equation which translates the charge of the capacitance C is written as:

10
$$\frac{\Delta Vc}{\Delta t} = \frac{1}{C} \times \frac{\mu \times Cox}{2} \times \frac{W}{L} \times \left(\frac{Re}{Rg2} \right)^2 \times K2^2 \times Vg2^2.$$

The presence of the resistance Re advantageously permits compensation for the variations of the resistance $Rg2$. The resistances Re and $Rg2$ are chosen to be of the same type of technology, thereby
15 allowing compensation for their spreads.

It is then possible, for example, to obtain a variation of the gradient $\frac{\Delta Vc}{\Delta t}$ on the order of $\pm 25\%$ for a variation of resistances $Rg2$ and Re , each on the order of $\pm 40\%$ in total. The resistance Re is
20 preferably chosen with a temperature variation coefficient of the same order of magnitude as that for the resistance $Rg2$. It is then possible to compensate for variations in temperature due to the resistance $Rg2$. Preferably, as has been previously mentioned, the

25 voltage V_{g2} is proportional to the quantity $k\frac{T}{q}$. The

mobility of the carriers varies proportionately to $T^{-3/2}$.

It follows that the voltage ramp $\frac{\Delta V_c}{\Delta t}$ varies proportionately to $T^{1/2}$.

Figure 3 shows a current ramp generator according to the preferred embodiment of the invention. The current ramp generator includes a voltage ramp generator circuit such as that described in Figure 2, and a circuit that allows the voltage ramp to be converted into a current ramp.

The circuit allowing the conversion of the voltage ramp into a current ramp is made up of operational amplifier A, three transistors T1, T2, T3 and a resistance Rs. The three transistors T1, T2, T3 and the resistance Rs are connected as shown in Figure 1. Similarly, the first input (e-) of the operational amplifier A is connected to the source of transistor T1, the gate of which is connected to the output of the operational amplifier. The second input (e+) of the operational amplifier A is connected to a first terminal of the capacitance C. The second terminal of the capacitance C is connected to ground.

Since I_s is the current passing through transistor T3, the current ramp $\frac{\Delta I_s}{\Delta t}$ is written as:

$$\frac{\Delta I_s}{\Delta t} = \frac{1}{R_s} \times \frac{\Delta V_c}{\Delta t} ,$$

where $\frac{\Delta V_c}{\Delta t}$ is the voltage ramp such as that calculated in the description of Figure 2. Hence, all the advantages described for the voltage ramp generator circuit in Figure 2 are also advantages that relate to the current ramp generator according to the invention.

As has already been previously mentioned, the voltage ramp $\frac{\Delta V_c}{\Delta t}$ varies with temperature according to $T^{1/2}$.

In accordance with the preferred embodiment
5 of the invention, the resistance R_s is an implanted N-type resistance with a positive temperature variation coefficient that enables the temperature variation of the current ramp to vary according to T^n , where n is
less than $\frac{1}{2}$. To reduce the effect of component
10 variations on the ramp, the capacitance C is the gate capacitance of a MOS transistor, the spread of which compensates for the spread of transistor T_5 .

THAT WHICH IS CLAIMED:

1. A voltage ramp generator $\left(\frac{\Delta V_c}{\Delta t}\right)$ comprising
a capacitance (C) and a charging circuit for the
capacitance that permits generation of a charging
5 current for the capacitance (IT5), the charging circuit
for the capacitance comprising a current generator
(Ig2) of resistance Rg2, characterized in that the
charging circuit for the capacitance includes means
(Re, T4, T5) that enable the capacitance charging
10 current to be proportional to $(Re/Rg2)^2$ where Re is a
resistance.

2. A voltage ramp generator according to
Claim 1, characterized in that the circuit for charging
the capacitance is a degenerate current mirror type
circuit.

3. A voltage ramp generator according to
Claim 2 characterized in that the a degenerate current
mirror type circuit is made up of a first P-type MOS
transistor (T4) comprising a gate, a drain and a source
5 and a second P-type transistor (T5) comprising a gate,
a drain and a source, the source of the first
transistor (T4) being connected to the first terminal
of the resistance Re, the second terminal of which is
connected to a supply voltage (V+), the drain and the
10 gate of the first transistor (T4) being connected to a
first terminal of the current generator (Ig2), the
second terminal of which is connected to the ground of
the circuit, the gate, the source and the drain of the
second transistor (T5) being connected respectively to
15 the gate of the first transistor (T4), to the supply
voltage (V+), and to the first terminal of the
capacitance (C), the second terminal of which is
connected to the ground of a circuit.

4. A voltage ramp generator according to Claim 3, characterized in that the capacitance (C) is a gate capacitance of a MOS transistor.

5. A voltage ramp generator according to any one of Claims 1 to 4, characterized in that the current (Ig2) generated by the current generator is written:

5
$$I_{g2} = K_2 \times \frac{V_{g2}}{R_{g2}}$$

where Vg2 is a reference voltage,

proportional to the quantity $k \frac{T}{q}$, where k is the Boltzmann constant, T is absolute temperature and q is the charge of an electron.

10

6. A generator of a current ramp $\left(\frac{\Delta I_s}{\Delta t} \right)$

comprising a generator of a voltage ramp $\left(\frac{\Delta V_c}{\Delta t} \right)$ and a circuit that permits the conversion of the voltage ramp into a current ramp, characterized in that the voltage ramp generator is a voltage ramp generator according to any one of Claims 1 to 5.

7. A generator of a current ramp $\left(\frac{\Delta I_s}{\Delta t} \right)$

according to Claim 6, characterized in that the circuit that permits the conversion of the voltage ramp into a current ramp includes a resistance (Rs) that

allows the conversion of the voltage ramp $\left(\frac{\Delta V_c}{\Delta t}\right)$ into a
current ramp $\left(\frac{\Delta I_s}{\Delta t}\right)$.

8. A current ramp generator according to
Claim 7, characterized in that the resistance (R_s) that

allows the conversion of the voltage ramp $\left(\frac{\Delta V_c}{\Delta t}\right)$ into a

current ramp is an implanted resistance having a
5 positive temperature coefficient.

VOLTAGE RAMP GENERATOR AND CURRENT RAMP GENERATOR
INCLUDING SUCH A GENERATOR

Abstract of the Disclosure

A voltage ramp generator includes a capacitance and a charging circuit that permits generation of a charging current for the capacitance. The charging circuit for the capacitance includes a
5 current generator having a resistance R_{g2} . The charging circuit for the capacitance includes components, such as resistance R_e , that enables the capacitance charging current to be proportional to $(R_e/R_{g2})^2$. The voltage ramp generator is applicable to
10 circuits for DC voltage converters operating in a current mode.

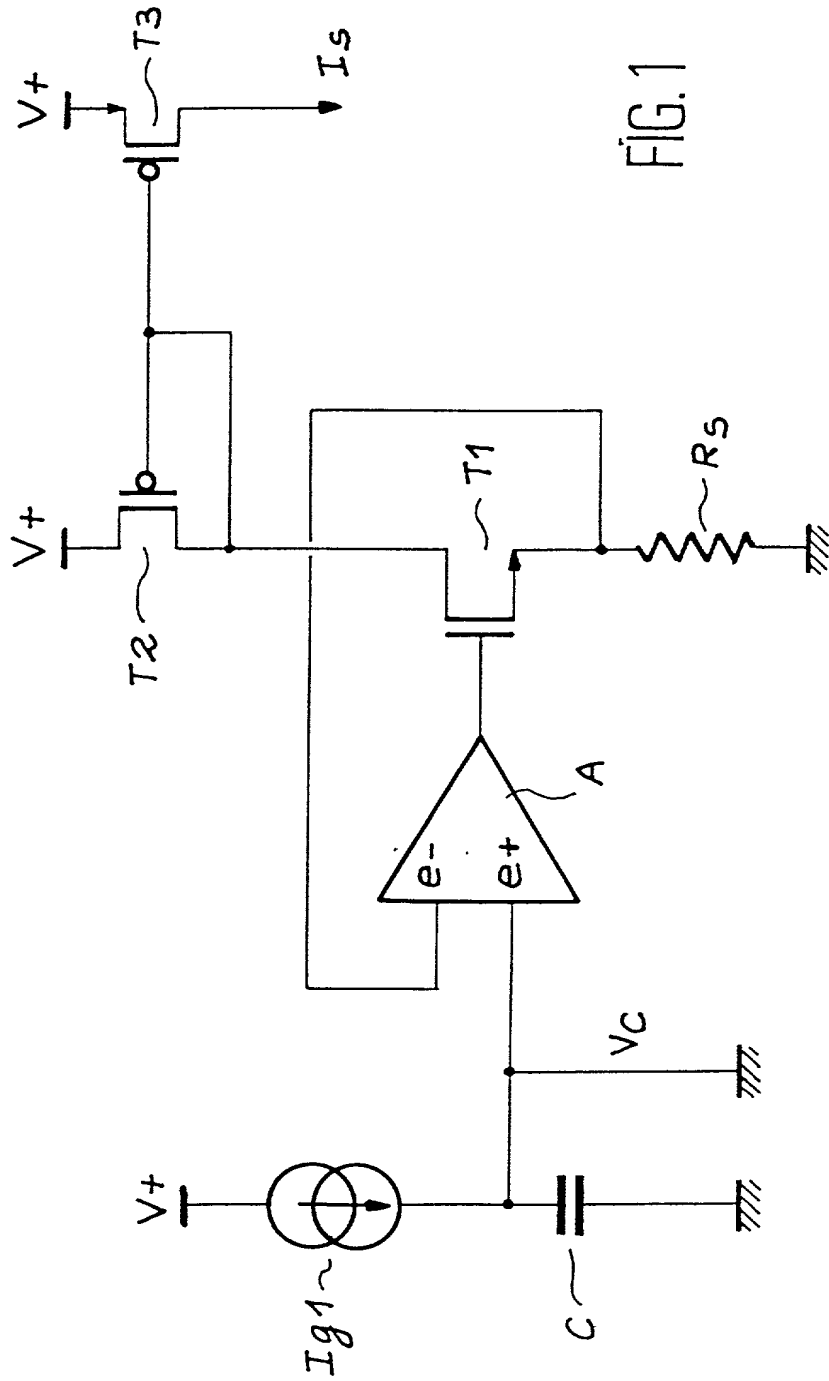
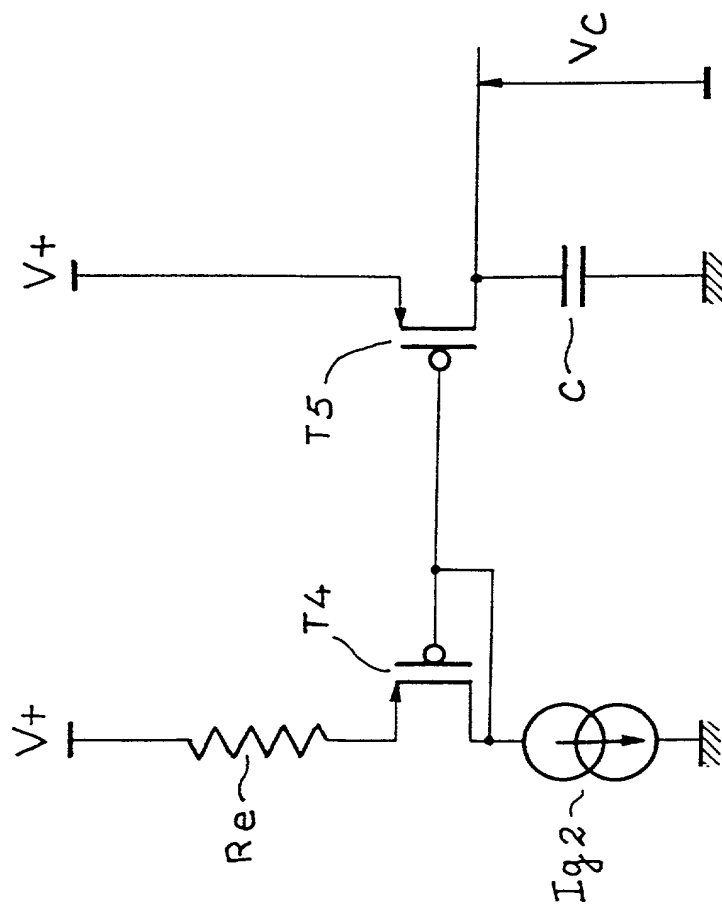


FIG. 1

FIG. 2



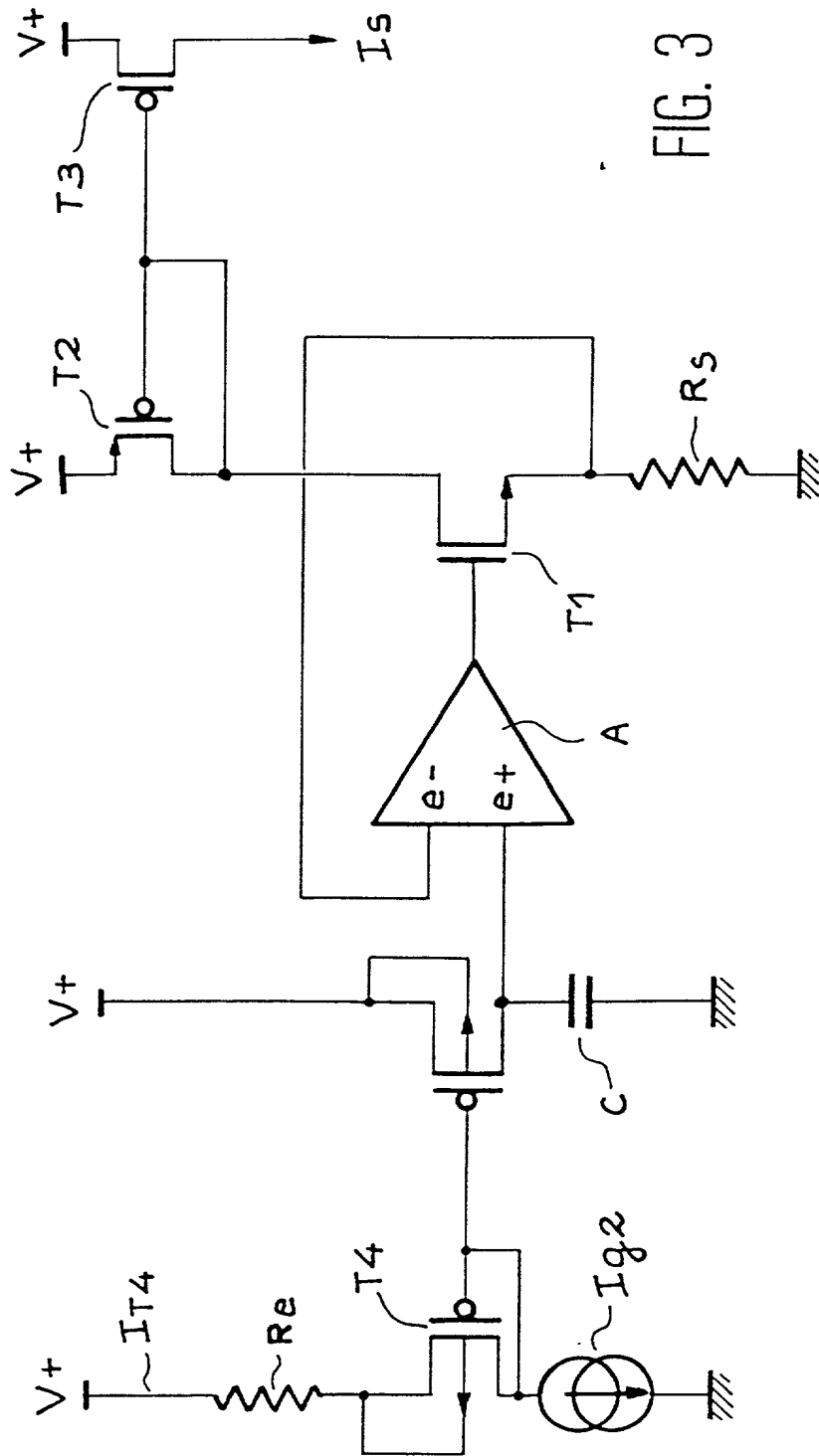


FIG. 3